



TFT LCD Approval Specification

MODEL NO.:V315H1-PH1

Customer: D-Long

Approved by: _____

Note:

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315H1-PH1 is a 31.5" TFT Liquid Crystal Display module. This module supports 1920* 1080

HDTV format and can display 1.073G colors (10bit/color).

1.2 CHARACTERISTICS

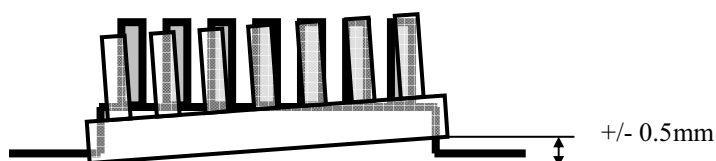
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	31.51
Pixels [lines]	1920*1080
Active Area [mm]	698.4 (H) x 392.85 (V) (31.51" diagonal)
Sub -Pixel Pitch [mm]	0.12125 (H) x 0.36375 (V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 1215
Physical Size [mm]	716.1(W) x 410(H) x 1.79(D) Typ.
Display Mode	Transmissive mode / Normally black
Contrast Ratio	4000:1 Typ. (Typical value measured at CMO's module)
Glass thickness (Array/CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H),+88/-88(V) Typ. (Typical value measured at CMO's module)
Color Chromaticity	R=(0.633, 0.322) G=(0.280, 0.607) B=(0.146, 0.055) W=(0.280, 0.290) (Typical value measured at CMO's module)
Cell Transparency [%]	4.6%Typ. (Typical value measured at CMO's module)
Polarizer (CF side)	Glare coating,Hard coating (3H) 709.7(H) x 405(w)..
Polarizer (TFT side)	Super Wide View, 709.7(H) x 405(w)..

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	1115	1215	1315	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within $\pm 0.5\text{mm}$ as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position





2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASED ON CMO MODULE V315H1-LH1)

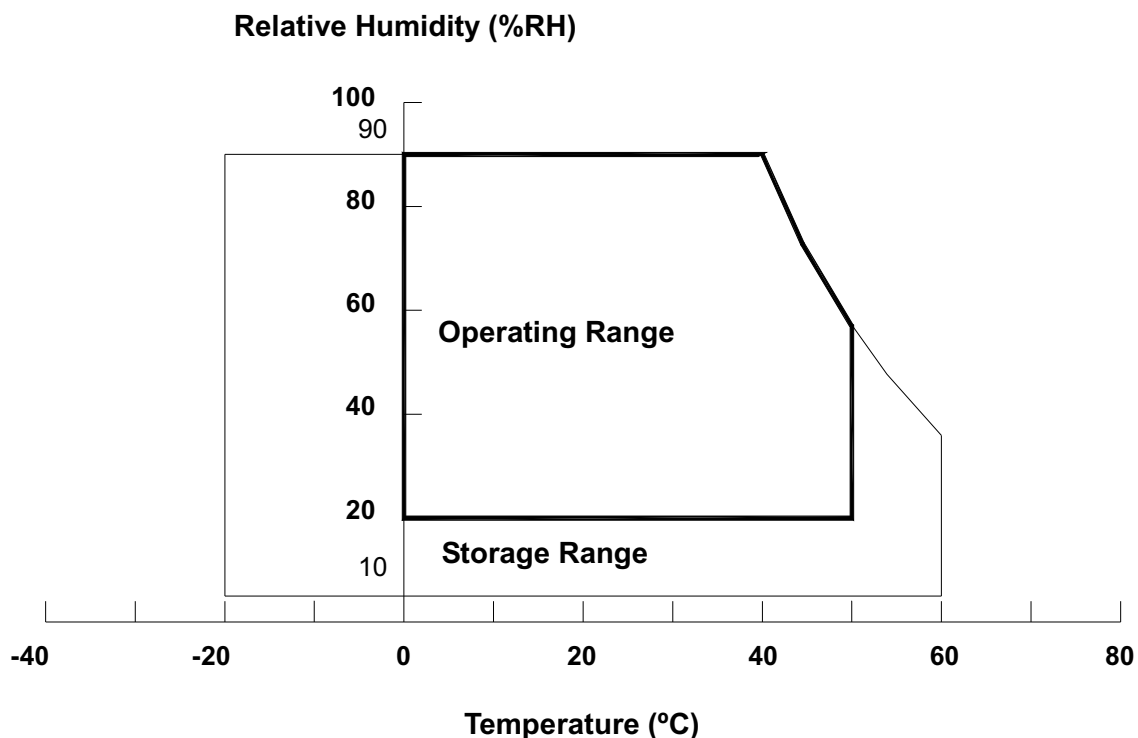
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1), (3)
Operating Ambient Temperature	T _{OP}	0	50	°C	(1), (2), (3)
Altitude Operating	A _{OP}	0	5000	M	(3)
Altitude Storage	A _{ST}	0	12000	M	(3)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

(c) No condensation..



Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Storage Condition : With shipping package.

Storage temperature range : $25\pm 5\text{ }^{\circ}\text{C}$

Storage humidity range : $50\pm 10\%\text{RH}$

Shelf life : a month

2.3 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)

Item	Symbol	Value		Unit	Note
		Min	Max		
Power Supply Voltage	VAA	-0.3	+18	V	(1)
Power Supply Voltage	VGH	-0.3	+31.0	V	
Power Supply Voltage	VGL	-8.3	-0.3	V	
Logic Input Voltage	V _{IN}	-0.3	3.4	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.



3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	VGHP	29	30	31	V	
	VGL	-8.3	-8	-7.7	V	
	VAA	17.4	17.7	18	V	
	V33V	3.2	3.3	3.4	V	
	VREF	16.7	17	17.3	V	
Power Supply Current	IGH	-	-	50	mA	
	IGL	-	-	50	mA	
	IAA	-	-	880	mA	
	I3.3V	-	-	2300	mA	
CMOS interface	V _{IH}	2.7	-	3.3	V	
	V _{IL}	0	-	0.7	V	

3.2 RSDS CHARACTERISTICS

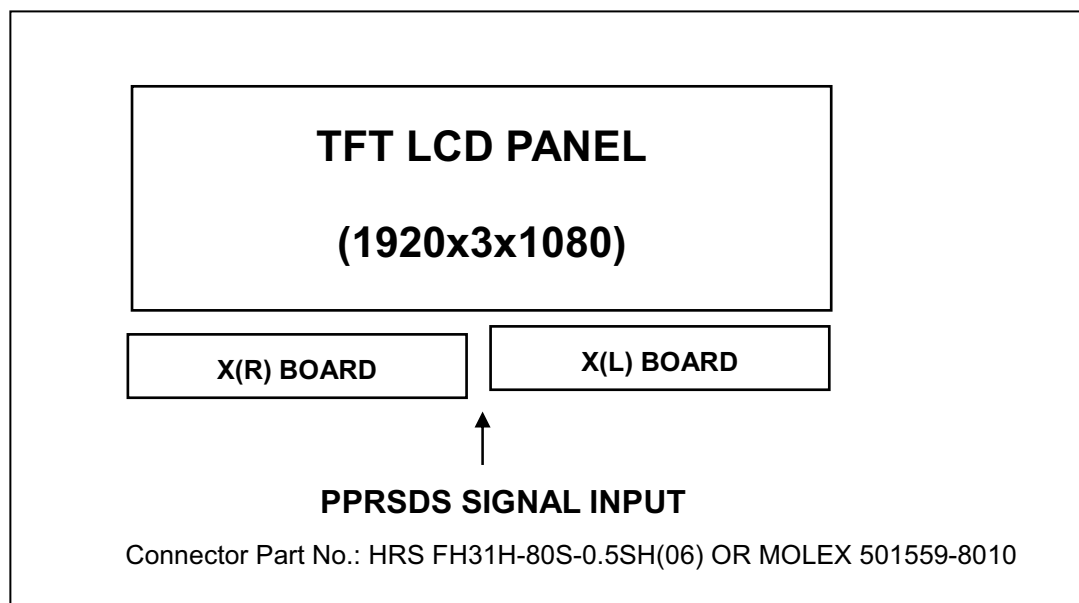
Ta = -10~+85 °C

Item	Symbol	Condition	Value			Unit
			Min	Typ	Max	
RSDS high input Voltage	V _{DIFFRSDS}	V _{CMRSDS} = +1.2 V (1)	100	200	-	mV
RSDS low input Voltage	V _{DIFFRSDS}	V _{CMRSDS} = +1.2 V (1)	-	-200	-100	mV
RSDS common mode input voltage range	V _{CMRSDS}	V _{DIFFRSDS} = 200 mV (2)	VSSD+0.5	Note(3)	VSSD-1.2	V
RSDS Input leakage current	I _{DL}	A/BDxxP, A/BDxxN, A/BCLKP, A/BCLKN	-10	-	10	μA

Note (1) V_{CMRSDS} = (VCLKP + VCLKN)/2 or V_{CMRSDS} = (VD_{xx}P + VD_{xx}N)/2Note (2) V_{DIFFRSDS} = VCLKP - VCLKN or V_{DIFFRSDS} = VD_{xx}P - VD_{xx}NNote (3) V_{CMRSDS} = 1.2V(VDDD = 3.3V)

4. BLOCK DIAGRAM

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

CN1(XL) Connector Pin Assignment

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	GND	Ground	41	AD0M_1	A-Path RSDS data signal
2	BD1P_4	B-Path RSDS data signal	42	GND	Ground
3	BD1M_4	B-Path RSDS data signal	43	GM20	Gamma Power supply
4	GND	Ground	44	GM19	Gamma Power supply
5	N.C.	No connection	45	GM18	Gamma Power supply
6	N.C.	No connection	46	GM17	Gamma Power supply
7	GND	Ground	47	GM16	Gamma Power supply
8	BD0P_4	B-Path RSDS data signal	48	GM15	Gamma Power supply
9	BD0M_4	B-Path RSDS data signal	49	GM14	Gamma Power supply
10	AD1P_4	A-Path RSDS data signal	50	GM13	Gamma Power supply
11	AD1M_4	A-Path RSDS data signal	51	GM12	Gamma Power supply
12	AD0P_4	A-Path RSDS data signal	52	GM11	Gamma Power supply
13	AD0M_4	A-Path RSDS data signal	53	GM10	Gamma Power supply
14	BD1P_3	B-Path RSDS data signal	54	GM9	Gamma Power supply
15	BD1M_3	B-Path RSDS data signal	55	GM8	Gamma Power supply
16	BD0P_3	B-Path RSDS data signal	56	GM7	Gamma Power supply
17	BD0M_3	B-Path RSDS data signal	57	GM6	Gamma Power supply
18	AD1P_3	A-Path RSDS data signal	58	GM5	Gamma Power supply
19	AD1M_3	A-Path RSDS data signal	59	GM4	Gamma Power supply
20	AD0P_3	A-Path RSDS data signal	60	GM3	Gamma Power supply
21	AD0M_3	A-Path RSDS data signal	61	GM2	Gamma Power supply
22	BD1P_2	B-Path RSDS data signal	62	GM1	Gamma Power supply
23	BD1M_2	B-Path RSDS data signal	63	GND	Ground
24	BD0P_2	B-Path RSDS data signal	64	TP1	RSDS data latch
25	BD0M_2	B-Path RSDS data signal	65	CKV	Scan driver clock
26	AD1P_2	A-Path RSDS data signal	66	OE1	Scan driver output enable 1
27	AD1M_2	A-Path RSDS data signal	67	OE2	Scan driver output enable 2
28	GND	Ground	68	STV	Scan driver start pulse
29	A_CLKP	Data driver clock	69	GND	Ground
30	A_CLKM	Data driver clock	70	VDD	Logic Power supply
31	GND	Ground	71	VDD	Logic Power supply
32	AD0P_2	A-Path RSDS data signal	72	VDDA	Driver Power supply
33	AD0M_2	A-Path RSDS data signal	73	VDDA	Driver Power supply
34	BD1P_1	B-Path RSDS data signal	74	VCM	VCM Power supply
35	BD1M_1	B-Path RSDS data signal	75	VCM	VCM Power supply
36	BD0P_1	B-Path RSDS data signal	76	VGL	Driver Power supply
37	BD0M_1	B-Path RSDS data signal	77	VGL	Driver Power supply
38	AD1P_1	A-Path RSDS data signal	78	VGH	Driver Power supply
39	AD1M_1	A-Path RSDS data signal	79	VGH	Driver Power supply
40	AD0P_1	A-Path RSDS data signal	80	GND	Ground

**CN2(XR) Connector Pin Assignment**

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	GND	Ground	41	BD1M_6	B-Path RSDS data signal
2	VGH	Driver Power supply	42	BD0P_6	B-Path RSDS data signal
3	VGH	Driver Power supply	43	BD0M_6	B-Path RSDS data signal
4	VGL	Driver Power supply	44	AD1P_6	A-Path RSDS data signal
5	VGL	Driver Power supply	45	AD1M_6	A-Path RSDS data signal
6	VCM	VCM Power supply	46	AD0P_6	A-Path RSDS data signal
7	VCM	VCM Power supply	47	AD0M_6	A-Path RSDS data signal
8	VDDA	Driver Power supply	48	BD1P_5	B-Path RSDS data signal
9	VDDA	Driver Power supply	49	BD1M_5	B-Path RSDS data signal
10	VDD	Logic Power supply	50	BD0P_5	B-Path RSDS data signal
11	VDD	Logic Power supply	51	BD0M_5	B-Path RSDS data signal
12	GND	Ground	52	GND	Ground
13	VSCM	VSCM Power supply	53	GM20	Gamma Power supply
14	TP1	RSDS data latch	54	GM19	Gamma Power supply
15	STV	Scan driver start pulse	55	GM18	Gamma Power supply
16	CKV	Scan driver clock	56	GM17	Gamma Power supply
17	OE2	Scan driver output enable 2	57	GM16	Gamma Power supply
18	OE1	Scan driver output enable 1	58	GM15	Gamma Power supply
19	GND	Ground	59	GM14	Gamma Power supply
20	BD1P_8	B-Path RSDS data signal	60	GM13	Gamma Power supply
21	BD1M_8	B-Path RSDS data signal	61	GM12	Gamma Power supply
22	BD0P_8	B-Path RSDS data signal	62	GM11	Gamma Power supply
23	BD0M_8	B-Path RSDS data signal	63	GM10	Gamma Power supply
24	AD1P_8	A-Path RSDS data signal	64	GM9	Gamma Power supply
25	AD1M_8	A-Path RSDS data signal	65	GM8	Gamma Power supply
26	AD0P_8	A-Path RSDS data signal	66	GM7	Gamma Power supply
27	AD0M_8	A-Path RSDS data signal	67	GM6	Gamma Power supply
28	GND	Ground	68	GM5	Gamma Power supply
29	C_CLKP	Data driver clock	69	GM4	Gamma Power supply
30	C_CLKM	Data driver clock	70	GM3	Gamma Power supply
31	GND	Ground	71	GM2	Gamma Power supply
32	BD1P_7	B-Path RSDS data signal	72	GM1	Gamma Power supply
33	BD1M_7	B-Path RSDS data signal	73	GND	Ground
34	BD0P_7	B-Path RSDS data signal	74	AD1P_5	A-Path RSDS data signal
35	BD0M_7	B-Path RSDS data signal	75	AD1M_5	A-Path RSDS data signal
36	AD1P_7	A-Path RSDS data signal	76	N.C.	No connection
37	AD1M_7	A-Path RSDS data signal	77	N.C.	No connection
38	AD0P_7	A-Path RSDS data signal	78	AD0P_5	A-Path RSDS data signal
39	AD0M_7	A-Path RSDS data signal	79	AD0M_5	A-Path RSDS data signal
40	BD1P_6	B-Path RSDS data signal	80	GND	Ground

Note (1) C_CN1、2 Connector Part No.: FH31H-80S-0.5SH(06), Hirose

**CN505 Connector Pin Assignment**

Pin No.	Symbol	Description
1	VIN	+12.0V power supply
2	VIN	+12.0V power supply
3	VIN	+12.0V power supply
4	VIN	+12.0V power supply
5	VIN	+12.0V power supply
6	NC	No connection
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	ODD_RIN0N	Negative transmission data of First pixel 0
11	ODD_RIN0P	Positive transmission data of First pixel 0
12	ODD_RIN1N	Negative transmission data of First pixel 1
13	ODD_RIN1P	Positive transmission data of First pixel 1
14	ODD_RIN2N	Negative transmission data of First pixel 2
15	ODD_RIN2P	Positive transmission data of First pixel 2
16	GND	Ground
17	ODD_RINCLKN	Negative of First clock
18	ODD_RINCLKP	Positive of First clock
19	GND	Ground
20	ODD_RIN3N	Negative transmission data of First pixel 3
21	ODD_RIN3P	Positive transmission data of First pixel 3
22	ODD_RIN4N	Negative transmission data of First pixel 4
23	ODD_RIN4P	Positive transmission data of First pixel 4
24	GND	Ground
25	EVEN_RIN0N	Negative transmission data of Second pixel 0
26	EVEN_RIN0P	Positive transmission data of Second pixel 0
27	EVEN_RIN1N	Negative transmission data of Second pixel 1
28	EVEN_RIN1P	Positive transmission data of Second pixel 1
29	EVEN_RIN2N	Negative transmission data of Second pixel 2
30	EVEN_RIN2P	Positive transmission data of Second pixel 2
31	GND	Ground
32	EVEN_RINCLKN	Negative of Second clock
33	EVEN_RINCLKP	Positive of Second clock
34	GND	Ground
35	EVEN_RIN3N	Negative transmission data of Second pixel 3
36	EVEN_RIN3P	Positive transmission data of Second pixel 3
37	EVEN_RIN4N	Negative transmission data of Second pixel 4
38	EVEN_RIN4P	Positive transmission data of Second pixel 4
39	GND	Ground
40	SCL_I	SEC define
41	SDA_I	SEC define
42	TCON_CHECK	SEC define
43	TST_PGM	SEC define
44	HSYNC	SEC define
45	LVDS_SEL	SEC define

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46	I2C_SCL	SEC define
47	FRC_NRESET	SEC define
48	I2C_SDA	SEC define
49	SW_PVCC	SEC define
50	MAIN_CHECK	SEC define
51	NC	No connection

Note (1) CN505 Connector Part No.: JAE Taiwan (台灣航空電子) FI-RE51S-HF or equal.


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5.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																														
		Red										Green										Blue										
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (1021)	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
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	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	-	74	-	MHZ	
Hsync		Fh	-	67.5	-	KHz	
Vsync		Fv	-	59.94	-	Hz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr6	57	60	63	Hz	
	Total	Tv	-	1125	-	Th	Tv=Tvd+Tvb
	Display	Tvd	-	1080	-	Th	-
	Blank	Tvb	-	45	-	Th	-
Horizontal Active Display Term	Total	Th	-	2200	-	Tc	Th=Thd+Thb
	Display	Thd	-	1920	-	Tc	-
	Blank	Thb	-	280	-	Tc	-

6.2 INTERNAL SIGNAL TIMING SPECIFICATIONS (FRC→ T-CON)

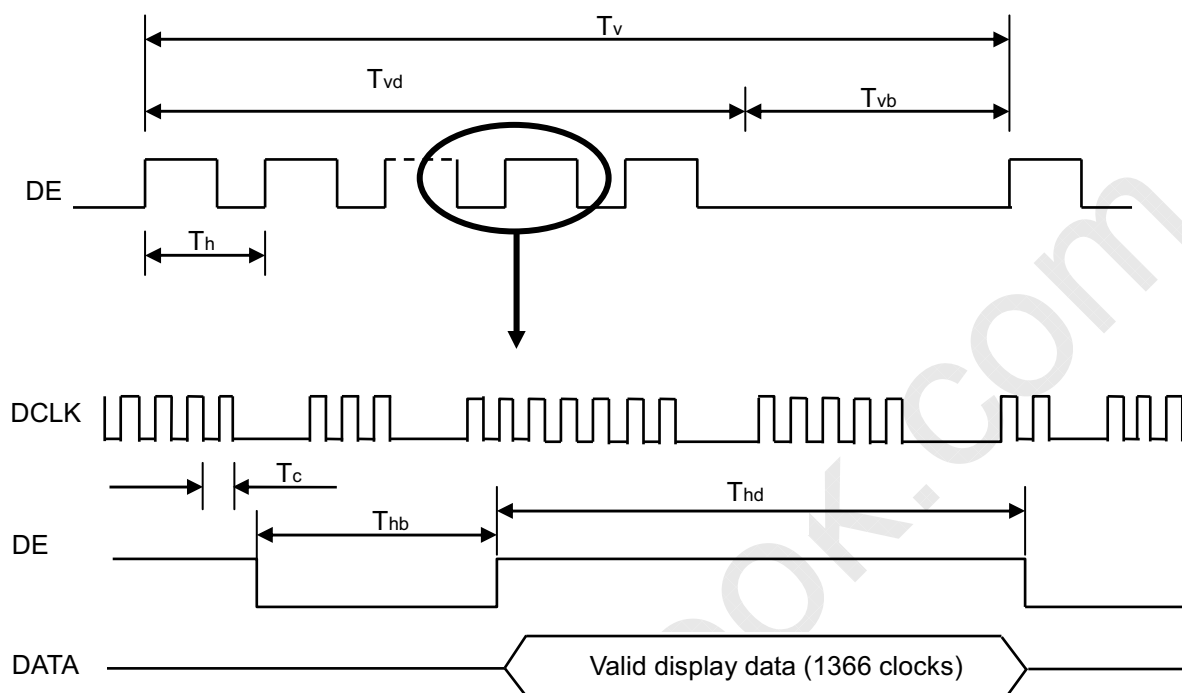
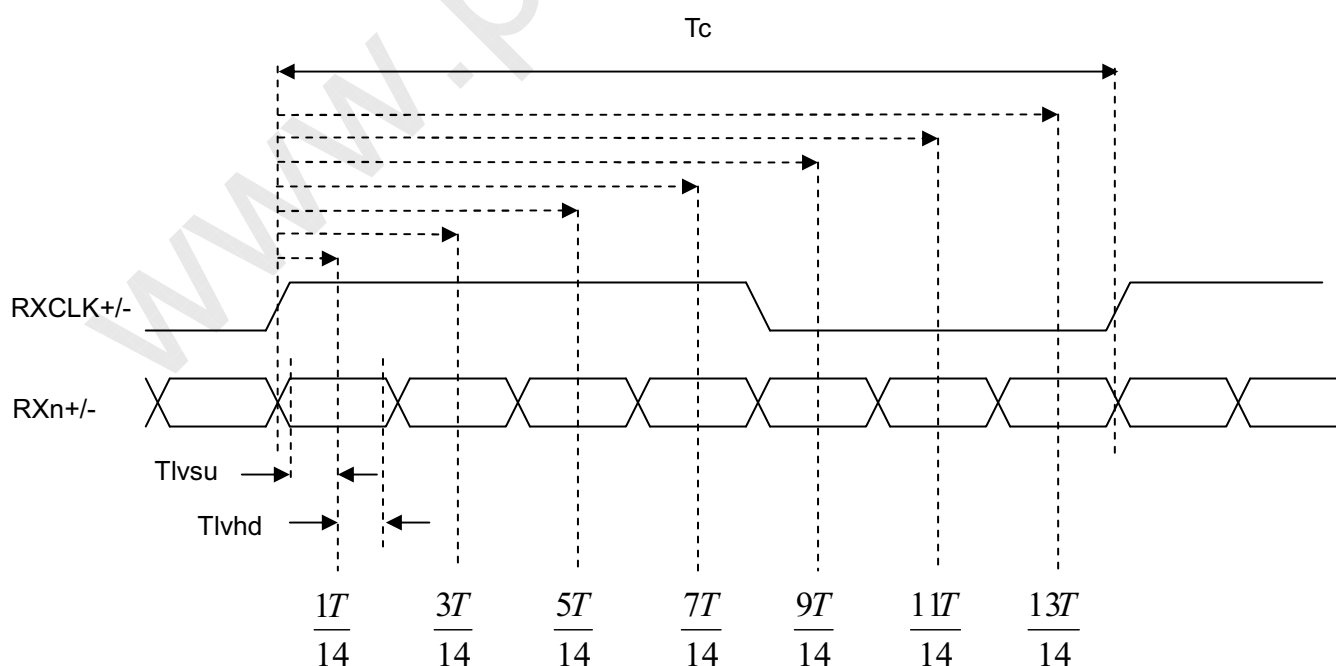
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHZ	(1)
Hsync		Fh	-	135	-	KHz	
Vsync		Fv	-	120	-	Hz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr6	-	120	-	Hz	
	Total	Tv	1115	1125	1410	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	330	Th	-
Horizontal Active Display Term	Total	Th	540	550	663	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	60	70	183	Tc	-

Note : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (1) LVDS Clock should not over 80MHz even if H-total or V-total is in spec, and the frequency follows the equation below.

$$\text{LVDS CLK} = \text{Frame rate} * \text{H-total} * \text{V-total}$$

**INPUT SIGNAL TIMING DIAGRAM****LVDS RECEIVER INTERFACE TIMING DIAGRAM**



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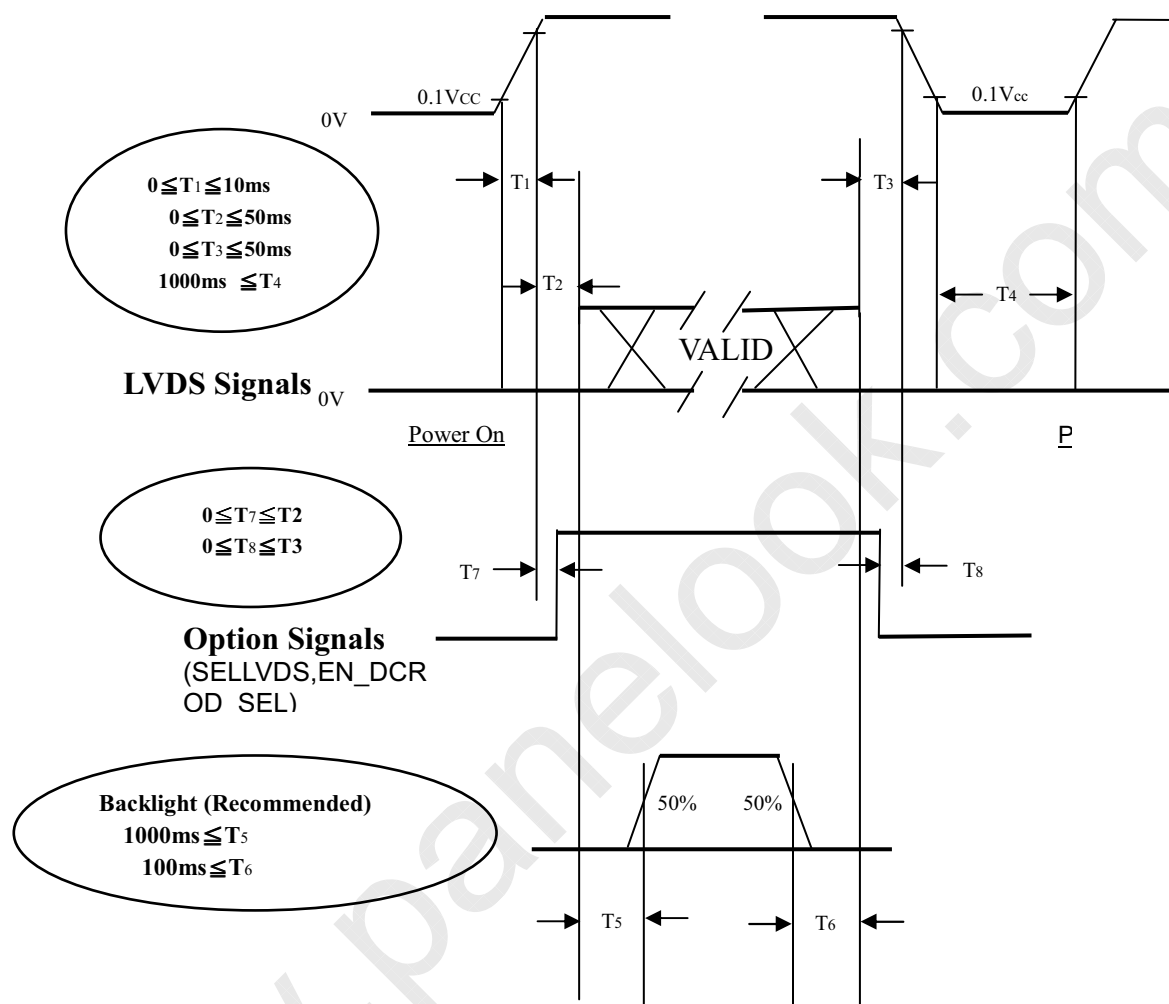
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6.3 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the conditions shown in the following diagram.



Power ON/OFF Sequence

Note.

- (1) The supply voltage of the external system for the module input should be the same as the definition of V_{CC}.
- (2) Please apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation of the LCD turns off, the display may, instantly, function abnormally.
- (3) In case of V_{CC} = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T₄ should be measured after the module has been fully discharged between power on/off periods.
- (5) Interface signal shall not be kept at high impedance when the power is on.



7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	5.2±0.5	mA
Inverter Driving Frequency	F _L	58±3	KHz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	R _x	θ _x =0°, θ _y =0° Viewing angle at normal direction With CMO module	Typ.-0.03	0.633	Typ+0.03	-	(1),(5)
		R _y			0.322		-	
	Green	G _x			0.280		-	
		G _y			0.607		-	
	Blue	B _x			0.146		-	
		B _y			0.055		-	
	White	W _x			0.280		-	
		W _y			0.290		-	
Center Transmittance		T%	θ _x =0°, θ _y =0° With CMO Module	-	4.6	4.6	%	(1), (7)
Contrast Ratio		CR		3000	4000	-	(1), (3)	
Response Time		Gray to gray average	θ _x =0°, θ _y =0° With CMO Module@120Hz	-	4.5	9	ms	(4)
White Variation		δW	θ _x =0°, θ _y =0° With CMO Module			1.3	-	(1), (6)
Viewing Angle	Horizontal	θ _x +	CR≥20 With CMO Module	80	88	-	Deg.	(1), (2)
		θ _x -		80	88	-		
	Vertical	θ _y +		80	88	-		
		θ _y -		80	88	-		

Note (1) Light source is CMO's V315H1-LH1 BLU and driving voltages are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by EZ-Contrast 160R (Eldim)

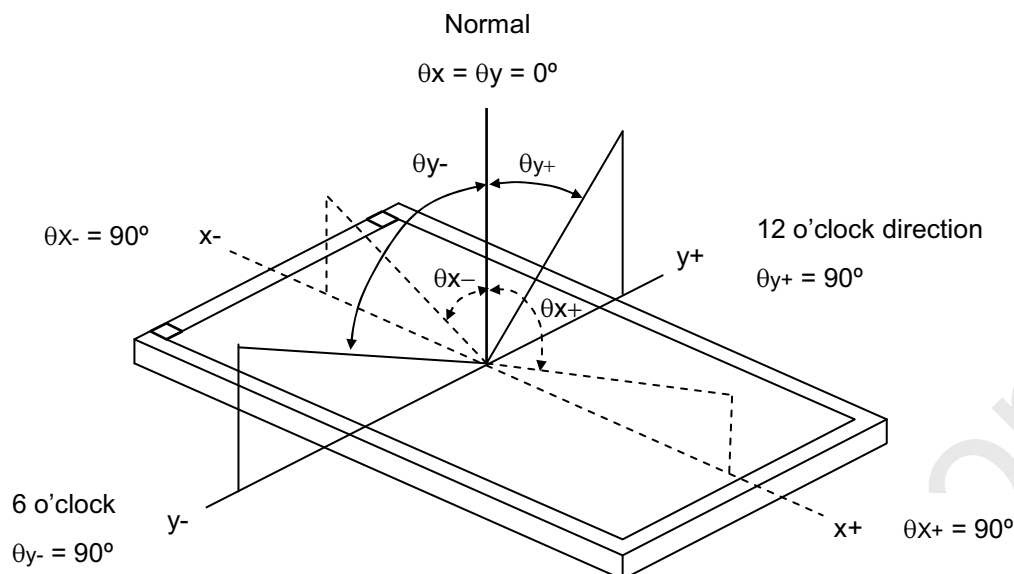


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Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

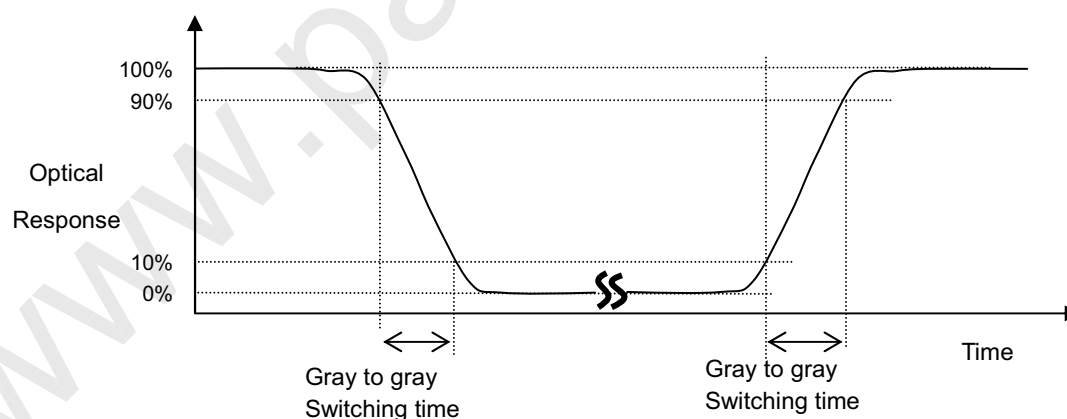
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5) ,where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of luminance 0%, 20%, 40%, 60%, 80%, 100%.

Gray to gray average time means the average switching time of luminance 0%,20%, 40%, 60%, 80%, 100% to each other.

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 60 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 60 minutes in a windless room.

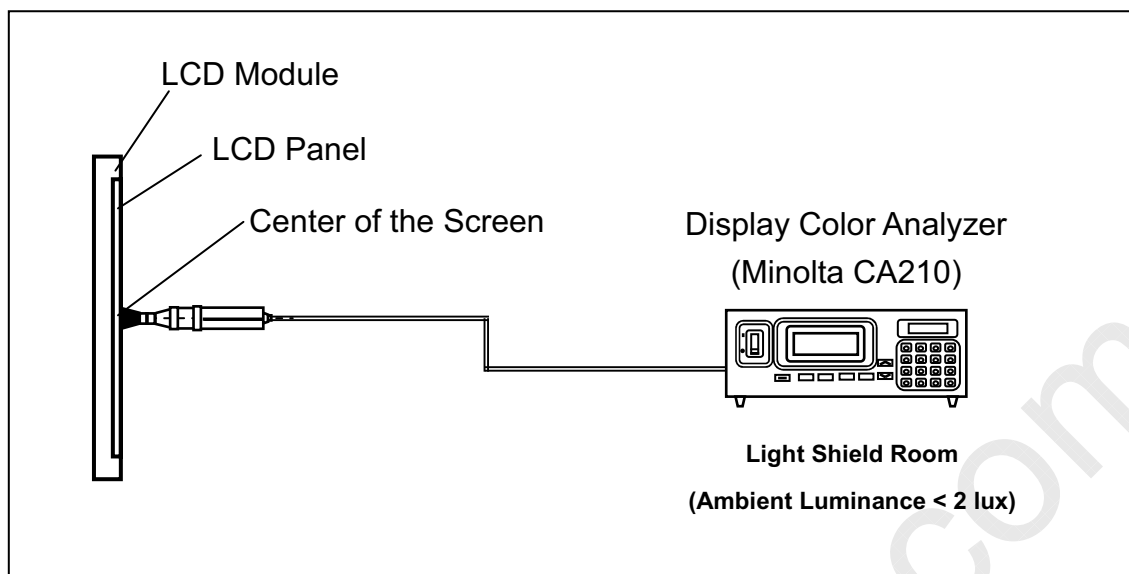


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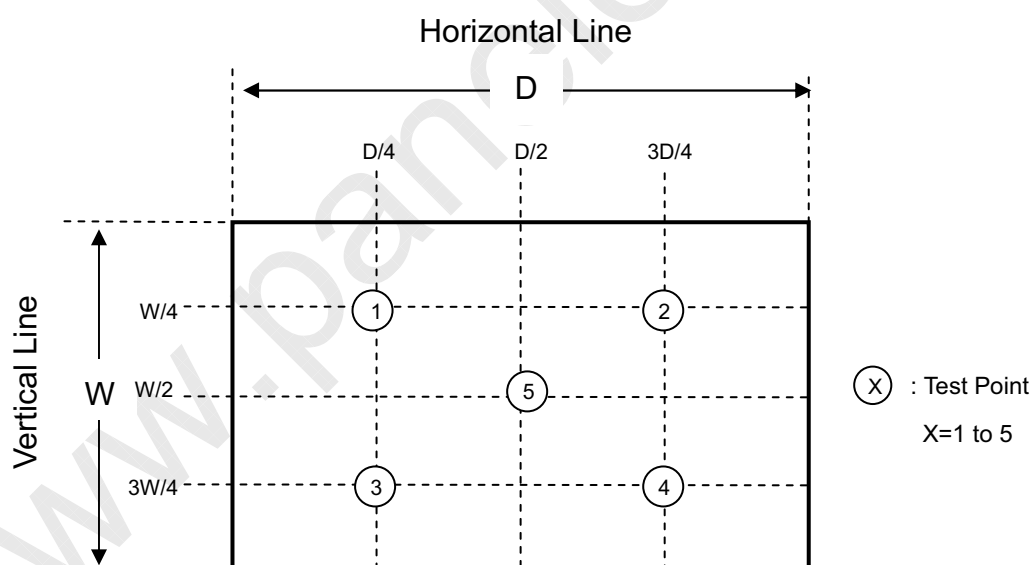


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$

where L (X) is corresponding to the luminance of the point X at the figure below.



Note (7) Definition of Transmittance(T%): Active Area

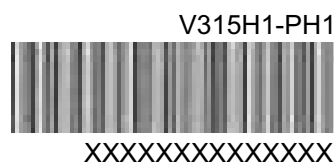
Module is without signal input.

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

8. DEFINITION OF LABELS

8.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMO internal control.



8.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

P.O. NO. _____	
Parts ID. _____	
Carton ID. _____	Quantities <u>21</u>
XXXXXXXXXXXXXXXX	
Made in Taiwan	

- (a) Model Name: V315H1– PH1
- (b) Carton ID: CMO internal control
- (c) Quantities:21

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 21 LCD TV Panels / 1 Box
- (2) Box dimensions : 970 (L) X 640 (W) X 319 (H)
- (3) Weight : approximately 38Kg (21 panels per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

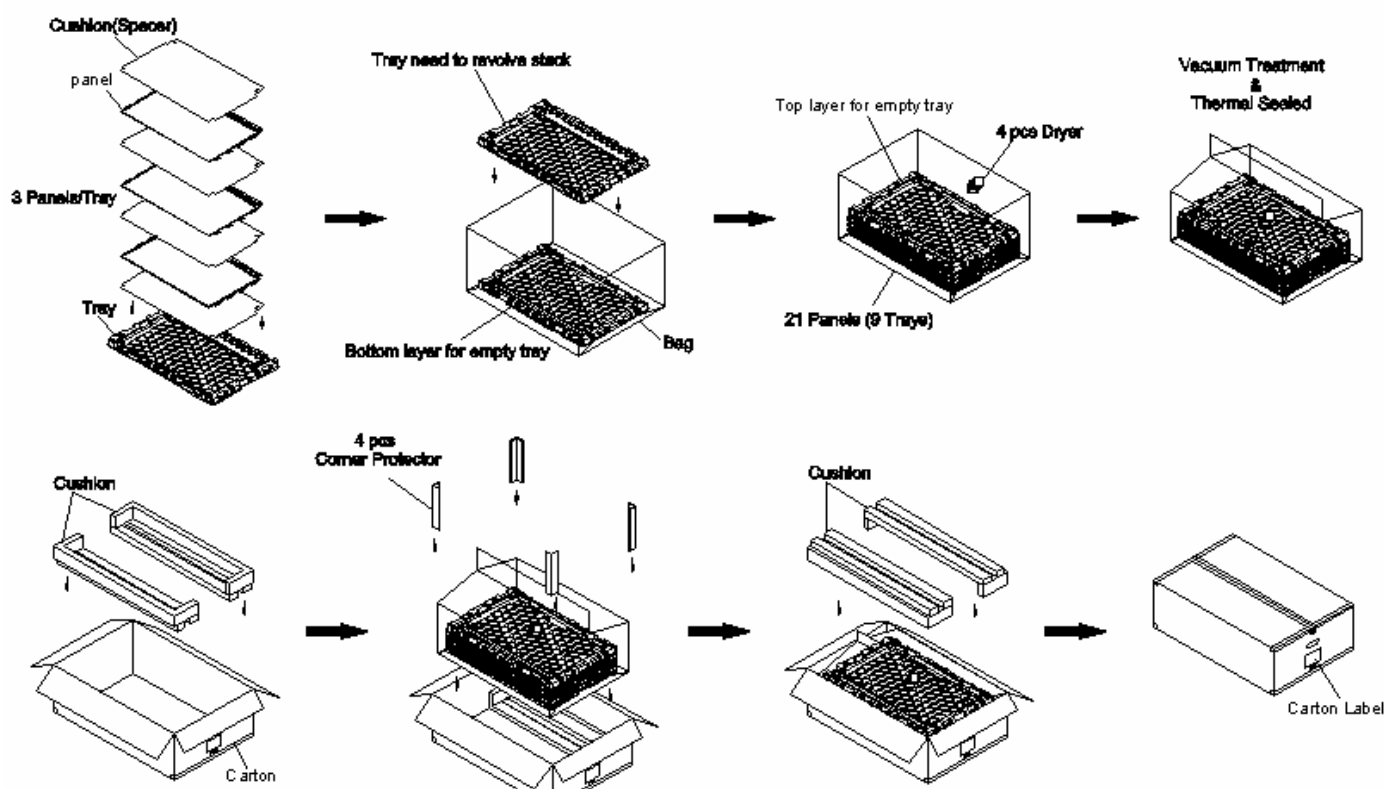


Figure.9-1 packing method



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Sea & Land Transportation

Gross : 471kg

Air Transportation

Gross : 319kg

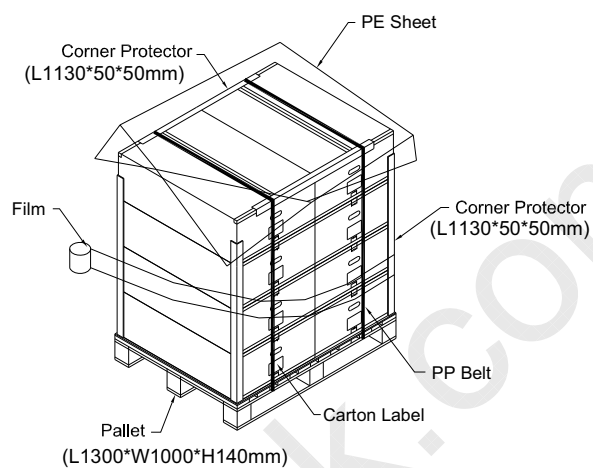
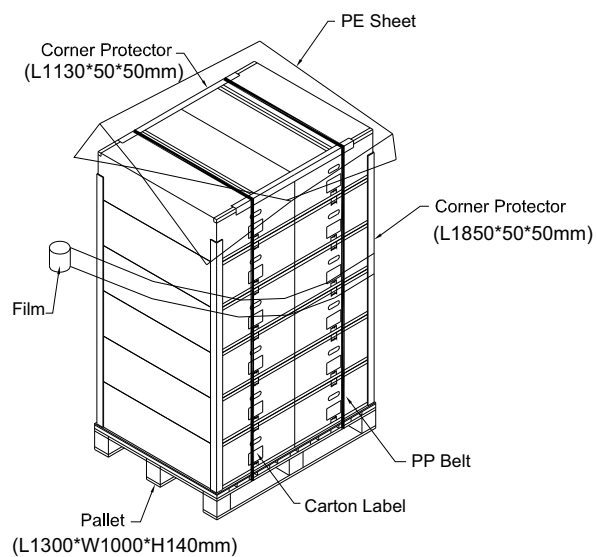


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the product during assembly.
- (2) To assemble backlight or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel will be damaged.
- (4) Always follow the correct power sequence when the product is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (7) It is dangerous that moisture come into or contacted the product, because moisture may damage the product when it is operating.
- (8) High temperature or humidity may reduce the performance of module. Please store this product within the specified storage conditions.
- (9) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly.

10.2 SAFETY PRECAUTIONS

- (1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (2) After the product's end of life, it is not harmful in case of normal operation and storage.

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